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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/551,266	09/29/2005	Toshiro Akino	9694D-000025/US	3385
30593 7590 03/03/2008 HARNESS, DICKEY & PIERCE, P.L.C. P.O. BOX 8910 RESTON, VA 20195			EXAMINER	
			O'TOOLE, COLLEEN J	
KESTON, VA	20193		ART UNIT	PAPER NUMBER
			2816	
			MAIL DATE	DELIVERY MODE
			03/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed February 11, 2008 have been fully considered but they are not persuasive. Applicant asserts that because NMOS transistors 321 and 323 merely supply substrate bias VBB2 and VBB3 according to control signals CNT and /CNT, respectively, 321 and 323 are used solely to bias the silicon substrate and cannot be considered current sources. Examiner respectfully disagrees. Transistors 321 and 323 inherently generate current when activated by the control signals CNT and /CNT. Therefore, NMOS transistors 321 and 323 fulfill the current source limitations recited in claim 1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to COLLEEN O'TOOLE whose telephone number is (571)270-1273. The examiner can normally be reached on M-F 8:30-5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/C. O./ Examiner, Art Unit 2816

> /QUAN TRA/ Primary Examiner, Art Unit 2816